Modeling And Analysis Of Induction Motor Drive With Novel Multilevel Inverter

K.Vinothini, M.Jagabar Sathik,Dr. K.Ramani

Abstract- Multilevel Inverter has been recognized as an attractive topology for high voltage DC-AC conversion. Multi-level inverters are also the best form to solve power quality problems. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. This paper presents a modified Cascaded H-Bridge Multilevel Inverter with reduction of power switches with the combined high and low switching frequencies. Feasibility of the developed approach has been identified with the optimum number of switches for electrical drives applications. In this paper, a detailed d-q modeling of a modified H-bridge multilevel VSI fed induction motor drive is developed. The simulation results are verified by using the Matlab/simulink 2009.

Index Terms- *cascaded H- bridge, Induction Motor Drive, Multilevel inverter, Modeling, Phase disposition(PD), SPWM technique, THD.*

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1 INTRODUCTION

Since the Multilevel inverter introduced in 1981 by Nabea, it establish a vital research area in the power electronics. Multilevel inverter is an effective solution for increasing power and reducing harmonics of ac waveforms. A multilevel inverter has an advantages over the conventional bipolar inverter are: reduced voltage stress, lower harmonic distortion, lower acoustic noise and electromagnetic interference (EMI) [1-5].

Now a day's multilevel inverters for motor drive applications of industry has become very popular. It is due to their high-power, high voltage capacity, low switching loss and low cost. In industrial applications three different major multilevel converter structures have been applied: Neutral Point Clamped, flying capacitors and cascaded H-bridge. Among them, the cascaded multilevel inverter is the most popular one [8]. It presents a number of attractive characters such as circuit layout is simple, reduced number of components, provides good modularity and avoids unbalance capacitor voltage problem. Though the number of power devices will get increases and the circuit becomes bulky when the number of output level gets increased [8]. In this paper, it is proposed to employ a new structure to obtain with a less number of switches for multilevel output as compared to the conventional multilevel inverter.

Inverters are used to control the fundamental frequency and the magnitude of the ac output voltage in many applications. AC loads may require constant or adjustable voltage at their input terminals, when such loads are fed by inverters, it is essential that the output voltage of the inverters is so controlled as to fulfill the requirement of the loads [6]. In recent days, compare to DC machines AC machines are preferable due to their simple and most robust

construction without any mechanical commutators. Induction motors are the most widely used motors for appliances like industrial control, and automation; hence, they are often called the workhorse of the motion industry[7]. As far as the machine efficiency, robustness, reliability, durability, power factor, ripples, stable output voltage and torque are concerned, three- phase induction motor stands at the a top of the order. Due to its distinguished advantages of easy construction as well as low cost machine, the induction motor accepted in variable speed drives. It needs maintenance or replacement for some internal parts [8]. In this work modelling of a proposed multilevel inverter with the induction motor was developed.

2. PROPOSED MULTILEVEL INVERTER

In this topology, it is divided into two parts (i) H Bridge (ii) Subsidiary Switches. The proposed topology for seven level is shown in Fig.1.The proposed topology has a parallel operation of high and low switching frequencies where the conventional H-bridge inverter for polarity changer which is normally called as low switching frequency section and the subsidiary switches (S_S) aid to obtain the multi stepped waveform which is operated in high switching frequency. The DC sources as the input V_{dc1} to V_{dcn} are independent and equal source voltages. By increasing number of level by one level the subsidiary switches, carrier signal and dc source will also increase by one.

The Generalized Equations

$$M = 2N_s + 1 \qquad -(1)$$

$$S_{Switch} = \left[\left(\frac{(M-1)}{2} \right) + 4 \right] \qquad -(2)$$

$$S_s = N_s \qquad -(3)$$

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- *Vinothini.k is currently pursuing masters degree program in power electronics and drive in J.J.college of engineering and technology,Trichy, Mobile-+91 9842815575. E-mail: yazhiniravi91@gmail.com*
- *Jagabar sathik.M. is currently working as an Asst.Professor (SE.G) in Department of Electrical and Electronics Engineering, JJ College of Engineering and Technology, Trichy, Mobile-+91 9500525422. E-mail: jagabarsathik@gmail.com*

Where M is the number of output voltage level, N_s number of DC sources, S_s a subsidiary switches and N_{switch} Number of Switch required.
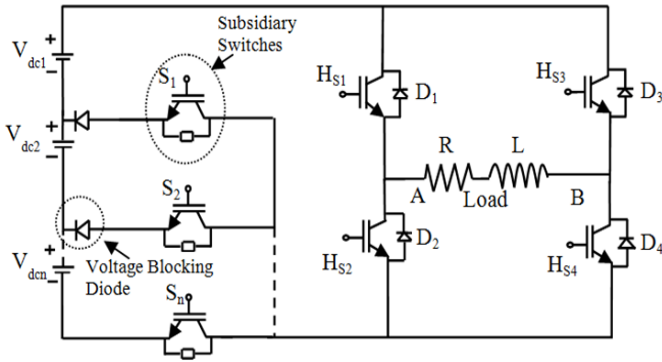

Fig.1.Generalized Structure of Proposed Topology

Table.1.The Switching Sequence for Seven Levels Output

Switches / Levels	H_{S1}	H_{S2}	H_{S3}	H_{S4}	S_1	S_2	S_3	Voltage Level
Positive Cycle Stepped Levels	1	0	0	1	1	0	0	$+V_{dc1}$
	1	0	0	1	0	1	0	$+V_{dc2}$
	1	0	0	1	0	0	1	$+V_{dc3}$
Zero State	0	0	0	0	0	0	0	0
	1	0	1	0	0	0	0	
Negative Cycle Stepped Levels	0	1	1	0	1	0	0	$-V_{dc1}$
	0	1	1	0	0	1	0	$-V_{dc2}$
	0	1	1	0	0	0	1	$-V_{dc3}$

The most attractive features of multilevel inverters are as follows:

- The advantages over conventional multilevel inverter in terms of reduced number of main switches, control circuits and it can provide good modularity.
- Switches gets reduced so switching and the conduction losses will be reduced.
- dv/dt Stress on the switching device are decreased.
- Optimum switching states for m-levels inverter.
- The Total harmonic distortion(THD) and the EMI will highly reduced.
- Compare to proposed topology some of the other topologies suffer from the additional components, complexities of capacitor balancing etc.

- The construction of proposed method is very simple and easy to replace the switches under failure conditions.
- In this topology less active state in each subsidiary switches it may cause to reduce the conduction losses and increase the life of the switches.

3. MODELING

Modeling of the proposed system

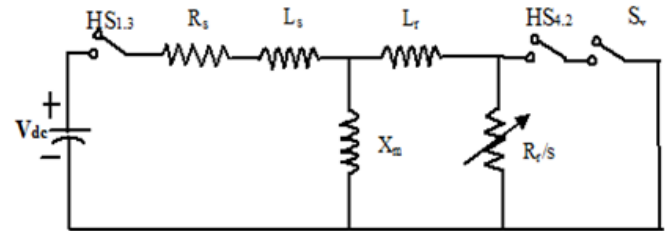The equivalent circuit of the proposed inverter is,

Fig.2. Equivalent Circuit of Proposed Topology

The State space equations illustrate the dependency of the switches, input and output equations. S(t) is Switching function w.r.t time. The state Space representation of the above circuits is,

$$i_1 R_1 + L_1 \frac{di_1}{dt} = V_{dc} * S(t) \quad -(4)$$

$$i_2 R_2 + L_2 \frac{di_2}{dt} = V_{dc2} * S(t) \quad -(5)$$

$$i_2 R_2 + L_3 \frac{di_3}{dt} = V_{dc3} * S(t) \quad -(6)$$

The general form of expression which states the switching sequence equation which relies on the V_{dc} is as follows.

(i). **Positive Cycle:** The state space equation can be written as

$$S_n(t) = \sum_{n-1}^{\frac{no.of levels-1}{2}} -\frac{R^3}{L^2} * i_n * \frac{1}{nV_{dc}} \quad -(7)$$

(ii).**Negative Cycle**: The state space equation can be written as

$$S_n(t) = \sum_{n-1}^{\frac{no.of levels-1}{2}} \frac{R^3}{L^2} * i_n * \frac{1}{nV_{dc}} \quad -(8)$$

Where n= 0, 1, 3, 5.... M

The three phase current are expressed as,

$$i_{an} = \left(L^2 * V_{dc} * sin(\omega t)\right)/\left(n * R^3\right) \qquad -(9)$$

$$i_{bn} = \left(L^2 * V_{dc} * sin(\omega t - (2\,\Pi/3))\right)/\left(n * R^3\right) \quad -(10)$$

$$i_{cn} = \left(L^2 * V_{dc} * sin(\omega t + (2\,\Pi/3))\right)/\left(n * R^3\right) \quad -(11)$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ \dfrac{1}{\sqrt{3}} & \dfrac{2}{\sqrt{3}} & 0 \end{bmatrix} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} \qquad -(12)$$

$$i_d = -\left(L^2 * V_{dc} * sin(\gamma - \omega t)\right)/\left(n * R^3\right) \quad -(13)$$

$$i_q = -\left(L^2 * V_{dc} * cos(\gamma - \omega t)\right)/\left(n * R^3\right) \quad -(14)$$

Modeling of Induction Motor Drive:

Voltage equation of induction motor in arbitrary reference frame[9] is

$$\begin{bmatrix} V_{qs}^a \\ V_{ds}^a \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + L_s p & \omega_a L_s & L_m p & \omega_a L_m \\ -\omega_a L_s & R_s + L_s p & -\omega_a L_m & L_m p \\ L_m p & (\omega_a - \omega_0) L_m & R_r + L_r p & (\omega_a - \omega_0) L_r \\ -(\omega_a - \omega_0) L_m & L_m p & -(\omega_a - \omega_0) L_r & R_r + L_r p \end{bmatrix} \begin{bmatrix} I_{qs}^a \\ I_{ds}^a \\ I_{qr}^a \\ I_{dr}^a \end{bmatrix} -(15)$$

For stationary reference frame, by substituting $\omega_a = 0$, the above equation is reduced[9,10] to

$$\begin{bmatrix} V_{qs}^s \\ V_{ds}^s \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + L_s p & 0 & L_m p & 0 \\ 0 & R_s + L_s p & 0 & L_m p \\ L_m p & -\omega_0 L_m & R_r + L_r p & -\omega_0 L_r \\ \omega_0 L_m & L_m p & \omega_0 L_r & R_r + L_r p \end{bmatrix} \begin{bmatrix} I_{qs}^s \\ I_{ds}^s \\ I_{qr}^s \\ I_{dr}^s \end{bmatrix} -(16)$$

Moreover, for synchronous frame, we have

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + L_s p & \omega_e L_s & L_m p & \omega_e L_m \\ -\omega_e L_s & R_s + L_s p & -\omega_e L_m & L_m p \\ L_m p & \omega_r L_m & R_r + L_r p & \omega_r L_r \\ -\omega_e L_m & L_m p & -\omega_r L_r & R_r + L_r p \end{bmatrix} \begin{bmatrix} I_{qs} \\ I_{ds} \\ I_{qr} \\ I_{dr} \end{bmatrix} -(17)$$

As mentioned before, each variable (voltage, current or flux linkage) in the synchronous frame is stationary and fixed to a constant magnitude in steady-state [9]. Based on the synchronous frame equation a dynamic d-q equivalent circuit is shown below
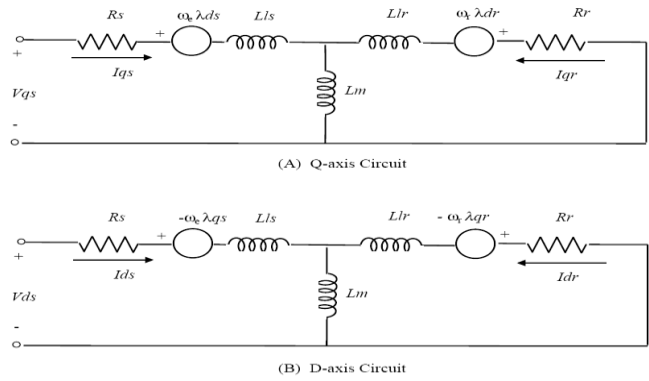

Fig.3. D-Q Equivalent Circuit on a Synchronous Frame

For dynamic simulation of induction motors, "(16)," or "(17)," may be used. In this case, one may prefer to use the standard form of differential equation as

$$\dot{X} = AX + BU \qquad -(18)$$

For "(17)," matrix quantities on the above equation are as follows.

$$X = \begin{bmatrix} I_{qs} \\ I_{ds} \\ I_{qr} \\ I_{dr} \end{bmatrix} \quad U = \begin{bmatrix} V_{qs} \\ V_{ds} \\ 0 \\ 0 \end{bmatrix} \quad B = 1/\Delta \begin{bmatrix} L_r & 0 & -L_m & 0 \\ 0 & L_r & 0 & -L_m \\ -L_m & 0 & L_s & 0 \\ 0 & -L_m & 0 & L_s \end{bmatrix}$$

And $\qquad\qquad -(19)$

$$A = 1/\Delta \begin{bmatrix} R_s L_r & \omega_e L_s L_r - \omega_r L_m^2 & -R_r L_m & \omega_0 L_m L_r \\ -\omega_e L_s L_r + \omega_r L_m^2 & R_s L_r & -\omega_0 L_m L_r & -R_r L_m \\ -R_s L_m & -\omega_0 L_s L_m & R_r L_s & \omega_r L_s L_r - \omega_e L_m^2 \\ \omega_0 L_s L_m & -R_s L_m & -\omega_r L_s L_r + \omega_e L_m^2 & R_r L_s \end{bmatrix}$$

In the above equation, $\Delta = L_s L_r - L_m^2$.

Combining "(13)," "(14)," "(18)" and "(19)" for adding The Induction Motor with The Inverter then the d-q axis current will be obtained as

$$I_q = -\frac{\left(L_r V_{qs} - I_{qr} L_m R_r + I_{qs} L_r R_s - I_{ds} L_m^2 \omega_r - I_{dr} L_m L_r \omega_0 + I_{ds} L_r L_s \omega_e\right)}{\left(L_m^2 - L_r L_s\right)}$$
$$-\frac{V_{dc} cos(\gamma - \omega_t)}{n} \qquad\qquad -(20)$$

$$I_d = -\frac{\left(L_r V_{ds} - I_{dr} L_m R_r + I_{ds} L_r R_s + I_{qs} L_m^2 \omega_r - I_{qr} L_m L_r \omega_0 - I_{qs} L_r L_s \omega_e\right)}{\left(L_m^2 - L_r L_s\right)}$$

$$-\frac{V_{dc} \sin\left(\gamma - \omega_t\right)}{n} \qquad -(21)$$

4. MODULATION TECHNIQUE:

Pulse width modulation techniques (PWM), introduced three decades ago, are the most used methods to control the voltage and frequency supplied to electrical AC machines. The sinusoidal pulse width modulation (SPWM) is one of the most popular modulation technique used in wide range of industrial application where power switching converters are employed[6]. The major reason for using multi-level inverters with PWM techniques is to improve the power quality and to reduce the harmonic content present in the power system networks. The two main advantages of PWM inverters in comparison to other inverters are (i) control over output voltage magnitude (ii) reduction in magnitudes of redundant harmonic voltages [6]. In SPWM technique carrier based modulation strategies are used. The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge(CHB) inverters.THD of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation. . There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation:

(i) In-phase disposition (IPD), where all carrier waveforms are in phase.

(ii) Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.

(iii)Alternate phase disposition (APOD), where every carrier waveform is in out of phase with its neighbor carrier by 180^0.

In this paper we are using Phase Disposition strategy for SPWM, which all the carriers are in phase as shown in fig.5. The rules for the in phase disposition method, when the number of level N = 7, are 1.The N –1 = 7-1=6 carrier waveforms are arranged so that every carrier is in phase. 2. The converter is switched to +Vdc when the reference is greater than both carrier waveforms. 3.The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform. 4.The converter is switched to - Vdc when the reference is less than both carrier waveforms.
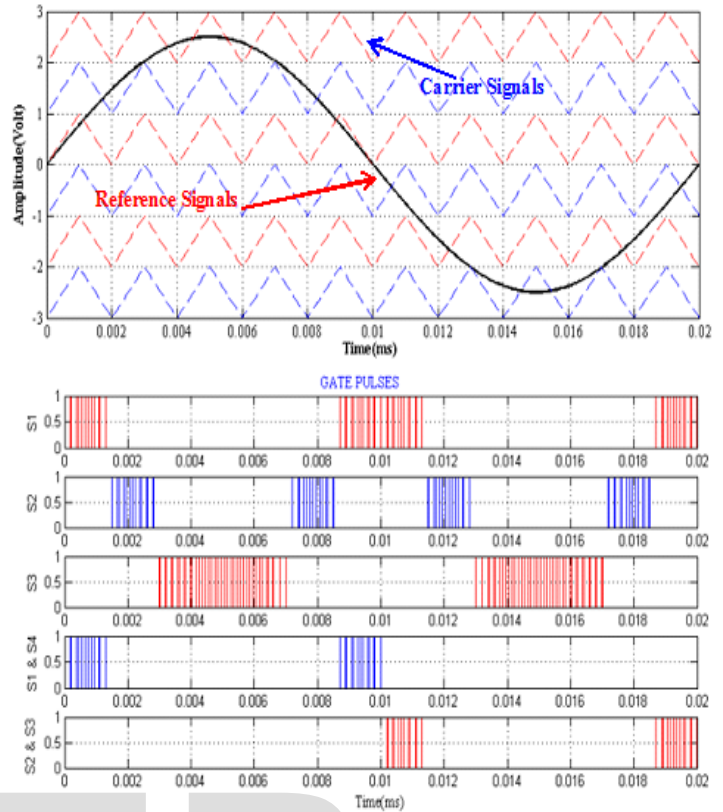

Fig. 4: Modulation Waveform of Phase Disposition PWM

5. SIMULATION RESULTS

The simulation of proposed multilevel inverter fed induction motor for seven level is developed using the Matlab/Simulink software. For generation of PWM pulses the technique was used comparing sinusoidal control voltage (at the desired output frequency and proportional to the output voltage magnitude) with a triangular waveform at a combination of high and low switching frequency. A 3-phase squirrel cage motor rated 3 HP, 220 V, 50 Hz, 1725 rpm is fed by a proposed inverter connected to a DC voltage source of 300 V. The proposed inverter is designed using the power devices & dc sources and the motor by the "Asynchronous Machine" block.

Fig.6. shows the inverter output voltage at 50HZ and the corresponding FFT plot normalized to the fundamental output voltage magnitude. It can be observed from the plot that the harmonics are limited and the THD is 13.71%.
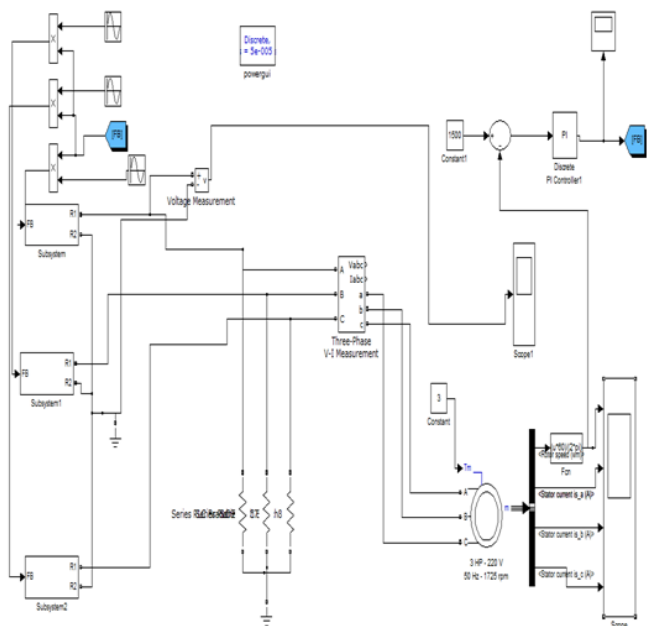
Fig.5.Simulink Model for open loop novel multilevel
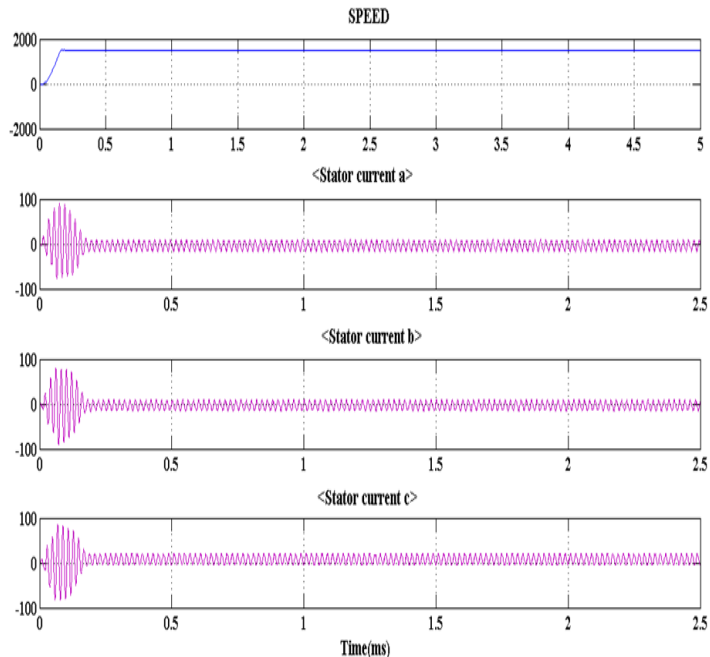Inverter fed Induction Motor Drive

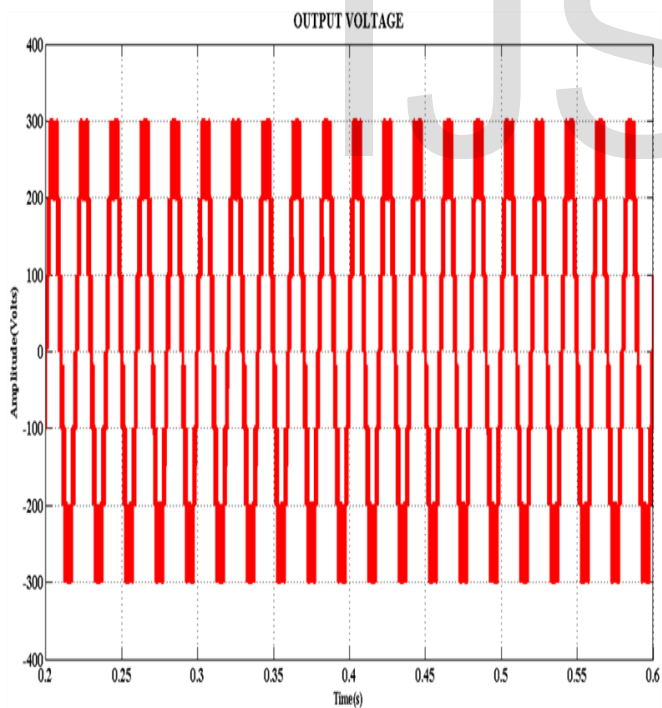Fig.7.Open loop speed and stator current versus time graph
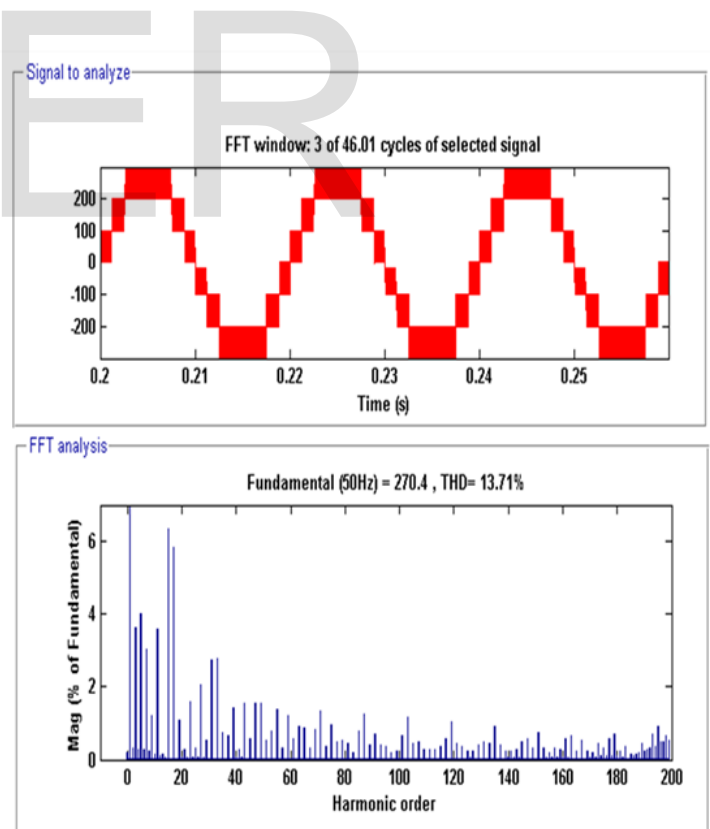

Fig.6.Output voltage versus time graph

Fig.8.FFT analysis of output voltage

CONCLUSION

This paper developed a modelling and analysis of novel multi-level inverter fed three phase induction motor drive. In this paper "A New Modified Cascade H-Bridge Multilevel inverter with reduced number of switches" produced higher output voltage level consisting of seven voltage levels. The THD value decreases, when increasing higher output voltage levels and also reduce the number of switches, cost, area required, protection circuit, cooling equipment, and driving circuit and also switching losses decreases, efficiency increases. The application can be AC drives, Non-conventional Energy Sources and FACTS devices etc. The outputs are verified by simulation model developed using the Matlab/Simulink software.

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BIBLIOGRAPHIES

K.Vinothini was born in Tamilnadu, India, on March 27, 1991. She received her B.E degree in Electrical and Electronics Engineering from Annamalai University, Chidambaram, in 2012; currently she is doing M.E degree in Power Electronics and drives from JJ College of Engineering and Technology, Trichy. Her current research interests include simulation of multilevel inverter, Ac drives, and Power converters.

M.Jagabar Sathik is Post graduated in 2004 from Anna University, Chennai. He is currently working as an Assistant Professor in the department of EEE at J.J College of Engineering and Technology, Trichy from January 2011 onwards. Currently he is pursuing Ph.D from Anna University, Chennai and he has presented 4 papers in various international conferences/Journals. His current research interests include Power Converters, AC Drives, FACTS and Optimization.

Dr.K.Ramani is graduated in 2004 from Bharathiar University, Coimbatore and post graduated in 2006 at Anna University, Chennai. He received his PhD from Anna University Chennai. He is currently working as an Associate Professor in the department of EEE at K.S.Rangasamy College of Technology, Tiruchengode from January 2006 onwards. He received the 2013 Young Teacher Award from the AICTE.He published more than 15 international/national conferences and journals. His research interests involve power electronics converters, modeling of induction motor and optimization techniques. He is guiding UG, PG Students. He is an ISTE, IETE member.